MULTIMEDIA UNIVERSITY

STUDENT ID NO

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |

# MULTIMEDIA UNIVERSITY

# FINAL EXAMINATION

**TRIMESTER 1, 2015/2016**

## EEN7016 – SEMICONDUCTOR DEVICES

(PSDC)

18 SEPTEMBER 2015
2.30 p.m - 5.30 p.m
( 3 Hours )

---

**INSTRUCTIONS TO STUDENTS**

1. This Question paper consists of 7 pages with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

**Physical constants**

| | |
|---|---|
| Electronic charge: | $e = 1.6 \times 10^{-19}$ C |
| Planck's constant: | $h = 6.63 \times 10^{-34}$ Js |
| Avagadro's number: | $N_A = 6.02 \times 10^{23}$ atoms mol$^{-1}$ |
| Permittivity in vacuum (free space): | $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm |
| Permeability in vacuum (free space): | $\mu_o = 4\pi \times 10^{-7}$ H/m |
| Free electron mass: | $m_o = 9.11 \times 10^{-31}$ kg |
| Boltzmann's constant: | $k = 1.3806 \times 10^{-23}$ J/K |
| Thermal voltage at 300K: | $V_t = kT/e = 0.0259$ V |
| Dielectric constant of Silicon at 300 K: | $\varepsilon_r = 11.7$ |
| Dielectric constant of Silicon dioxide at 300 K: | $\varepsilon_i = 3.9$ |
| Intrinsic carrier concentration of Silicon at 300 K: | $n_i = 1.5 \times 10^{10}$ cm$^{-3}$ |
| Electron affinity of Silicon at 300 K: | $\chi = 4.01$ V |

**List of Formulas**

$$\phi_f = \left(\frac{kT}{q}\right)\ln\left(\frac{N_A}{n_i}\right)$$

$$C = \frac{\varepsilon}{d}$$

$$\phi_S = \frac{qN_A W^2}{2\varepsilon_S}$$

$$\frac{1}{C_{\text{Total}}} = \frac{1}{C_A} + \frac{1}{C_B}$$

$$V_T = \left[\frac{\sqrt{2q\varepsilon_S N_A \phi_{S(inv)}}}{C_i}\right] + \phi_{S(inv)}$$

$$C = \frac{C_i}{\sqrt{1+\frac{2V_G}{V_\delta}}} \quad \text{where} \quad V_\delta = \frac{q\varepsilon_S d^2 N_A}{\varepsilon_i^2} = \frac{q\varepsilon_S N_A}{C_i^2}$$

$$I_{D(sat)} = \frac{1}{2}\frac{z}{L}\bar{\mu}C_i\left(V_G - V_T\right)^2$$

$$I_D = \frac{z\bar{\mu}C_i}{L}\left[\left(V_G - V_T\right)V_D - \frac{1}{2}V_D^2\right]$$

## List of Formulas

$$V_{bi} = \frac{k_B T}{e} \ln\left(\frac{N_a N_d}{n_i^2}\right) = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right)$$

$$\phi_{Fn} = \left(-k_B T/e\right)\ln\left(N_d/n_i\right)$$

$$\phi_{Fp} = \left(k_B T/e\right)\ln\left(N_a/n_i\right)$$

$$x_n = \left[\frac{2\varepsilon_S V_{bi}}{e}\left(\frac{N_a}{N_d}\right)\left(\frac{1}{N_a + N_d}\right)\right]^{1/2}$$

$$x_p = \left[\frac{2\varepsilon_S V_{bi}}{e}\left(\frac{N_d}{N_a}\right)\left(\frac{1}{N_a + N_d}\right)\right]^{1/2}$$

$$W = \left[\frac{2\varepsilon_s V_{bi}}{e}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2}$$

$$\mathrm{E} = \frac{-eN_d x_n}{\varepsilon_S} = \frac{-eN_a x_p}{\varepsilon_S}$$

$$W = \left\{\frac{2\varepsilon_s\left(V_{bi} + V_R\right)}{e}\left[\frac{N_a + N_d}{N_a N_d}\right]\right\}^{1/2}$$

$$x_n = \left[\frac{2\varepsilon_S\left(V_{bi} + V_R\right)}{e}\left(\frac{N_a}{N_d}\right)\left(\frac{1}{N_a + N_d}\right)\right]^{1/2}$$

$$x_p = \left[\frac{2\varepsilon_S\left(V_{bi} + V_R\right)}{e}\left(\frac{N_d}{N_a}\right)\left(\frac{1}{N_a + N_d}\right)\right]^{1/2}$$

$$n_B(0) = n_{BO}\exp\left(\frac{V_{BE}}{V_t}\right)$$

$$p_E(0) = p_{EO}\exp\left(\frac{V_{BE}}{V_t}\right)$$

$$np = n_i^{\,2}$$

$$\mathrm{E}_{\max} = -\left[\frac{2e\left(V_{bi} + V_R\right)}{\varepsilon_S}\left(\frac{N_a N_d}{N_a + N_d}\right)\right]^{1/2} = \frac{-2\left(V_{bi} + V_R\right)}{W}$$

**Continued…**

## Question 1

(a) Describe how a space charge region is formed under the thermal equilibrium conditions for an ideal PN junction. [4 marks]

(b) With appropriate labels, sketch the cross section of PN junction and its associated energy-band diagram for zero bias, reverse bias, and forward bias, respectively. [6 marks]

(c) Explain what is "Schottky barrier height" for a metal-semiconductor junction. [2 marks]

(d) Identify the type of metal-semiconductor contact (rectifying or ohmic contact) when a metal and an n-type semiconductor are joined with $\Phi_M > \Phi_S$, and $\Phi_M < \Phi_S$, respectively. The $\Phi_M$ is the work function for the metal while $\Phi_S$ is the work function for the n-type semiconductor. [2 marks]

(e) An abrupt silicon PN junction as given in Figure Q1 below at zero bias has acceptor concentrations, $N_a$, of $10^{16}$ $cm^{-3}$ for P region, and donor concentration, $N_d$, of $5x10^{14}$ $cm^{-3}$ for N region. Assuming the PN junction is placed under room temperature, T, of 300 K. Determine the followings for this junction:

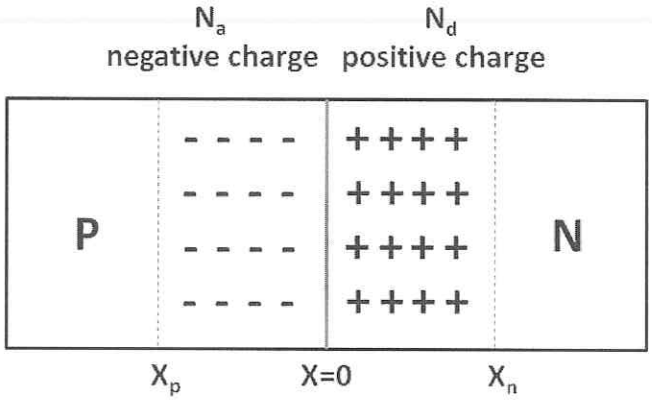


Figure Q1

(i) Fermi level on each side of the junction with respect to the intrinsic Fermi level ($E_{Fi} - E_{Fp}$ and $E_{Fn} - E_{Fi}$). [4 marks]

(ii) Built-in potential barrier, $V_{bi}$. [1 mark]

(iii) Widths of the depletion region extending into the n region, $x_n$, and p region, $x_p$. [4 marks]

(iv) Peak electric field. [2 marks]

**Continued...**

## Question 2

(a) Depending on the junction voltage conditions the bipolar junction transistors (BJTs) can be placed under four different types of operation modes.

(i) Identify these four types of operational modes for the BJTs. [4 marks]

(ii) Discuss the flow of carriers between the junctions for the BJTs under these four operational modes. [8 marks]

(b) A silicon npn BJT as given in Figure Q2 below is uniformly doped and biased in the forward active region. The neutral base width, $x_B$, is given as $0.8\mu m$. The transistor doping concentrations are $N_E = 10^{17}$ cm$^{-3}$, $N_B = 10^{15}$ cm$^{-3}$ and Nc = $10^{14}$ cm$^{-3}$, for emitter, base and collector regions, respectively.

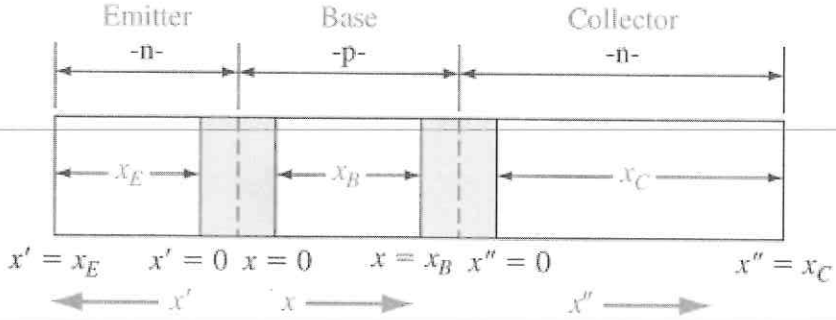


Figure Q2

(i) Determine the values of the thermal equilibrium minority carrier hole concentration in the emitter, $p_{EO}$, electron concentration in the base, $n_{BO}$, and hole concentrations in the collector, $p_{CO}$, respectively. [9 marks]

(ii) Determine the electron concentration in the base, $n_B$, at $x = 0$, and hole concentration in the emitter, $p_E$, at $x' = 0$, taking a base emitter voltage, $V_{BE}$, of 0.65V. [4 marks]

**Continued...**

## Question 3

(a) You are a device engineer. You are assigned to fabricate a metal-oxide-silicon (MOS) capacitor that exhibits capacitance-voltage (CV) characteristics as shown in Figure Q3. Given that intrinsic concentration, $n_i = 1.5\times10^{10}$ cm$^{-3}$; permittivity of silicon, $\varepsilon_s$ = 11.7; permittivity of silicon oxide, $\varepsilon_i$ = 3.9; permittivity of vacuum, $\varepsilon_o = 8.85\times10^{-14}$ Fcm$^{-1}$; electron charge, $q = 1.6\times10^{-19}$ C and thermal voltage, $kT/q$ = 0.0259 V.

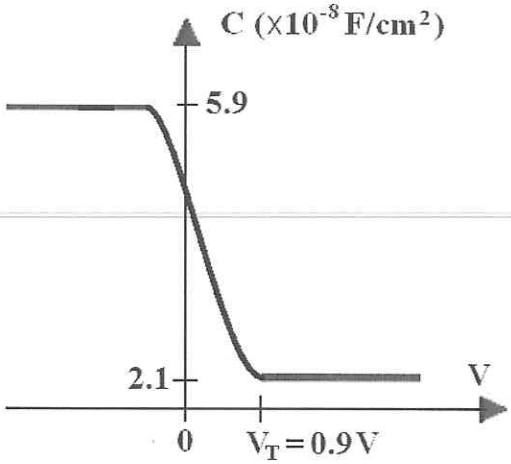


Figure Q3

(i) Suggest the type for silicon substrate and explain your answer. [2 marks]
(ii) Determine the thickness of oxide. [2 marks]
(iii) Determine the maximum value of depletion width. [4 marks]
(iv) Determine the doping concentration. [4 marks]

(b) In an ideal MOS capacitor system, charges are assumed in the semiconductor only. However, charges are induced in the semiconductor as well as semiconductor-insulator interface during real fabrication process. List **TWO** charges that induced during fabrication process and briefly explain these charges. [6 marks]

(c) An n-channel silicon MOSFET was fabricated with following parameters: channel width, z = 4μm; channel length, L = 1.2μm and oxide thickness, $t_{ox}$ = 10nm. When the transistor is biased in the saturation region, the drain current is $I_{D(sat)}$ = 0.15mA at gate voltage, $V_{GS}$ = 0.85V and $I_{D(sat)}$ = 0.24mA at $V_{GS}$ = 1.05V. Determine the electron mobility and the threshold voltage. [7 marks]

**Continued...**

## Question 4

(a) Reduction of device geometry has been shown to lead to major modifications of the device characteristics from that of the large-size or long-channel device. One of the phenomena is parasitic bipolar junction action. With suitable graphs and diagrams, briefly explain parasitic bipolar junction action. [9 marks]

(b) In complementary metal-oxide-semiconductor field effect transistor (CMOS) scaling, interconnection resistive-capacitive (RC) delay increases due to the complexity of the circuit. Due to this reason, materials with low dielectric constants, $k$, are used as interconnection isolation or passivation layer to reduce the interconnection RC delay. However, some issues are raised with the usage of low-$k$ materials. Discuss **TWO** issues in application of low-$k$ materials and the method to avoid each issue. [6 marks]

(c) As a device engineer, you are requested to apply heterostructure in devices to achieve better performance. The properties of Gallium Arsenide (GaAs) and Aluminum Gallium Arsenide ($Al_{0.4}Ga_{0.6}As$) are listed in Table Q4.

Table Q4

| Material | Bandgap | Conduction Band | Valence Band |
|---|---|---|---|
| GaAs | 1.42eV | 4.07eV | 5.49eV |
| $Al_{0.4}Ga_{0.6}As$ | 1.92eV | 3.63eV | 5.55eV |

(i) Construct the energy band diagram for a NPN heterojunction bipolar transistor (HBT) with GaAs and AlGaAs. Label clearly the material used for emitter, base and collector as well as their level of doping (high or low). Justify why those material or level doping are chosen. [5 marks]

(ii) Design the device structure of a high electron mobility transistor (HEMT) with GaAs and AlGaAs. Label clearly each layer of materials as well as the type of dopant. Summarize the operation of HEMT with energy band diagram of the heterojunction. [5 marks]

**End of Paper.**